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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,723	08/25/2003	Ken K. Foo	CS22497RA	2166

20280 7590 03/20/2007
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EXAMINER

KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
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2629

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/647,723	Applicant(s) FOO ET AL.	
	Examiner Vincent E. Kovalick	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-17, 19 and 20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5, 7-9, 17, 19 and 20 is/are allowed.
- 6) ☒ Claim(s) 1, 4, 10-12 and 16 is/are rejected.
- 7) ☒ Claim(s) 2, 3 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's Response, dated January 17, 2007, to USPTO Office Action dated October 17, 2006.

The cancellation of claims 6 and 18, the amendment to claim 7, and changing the dependency to claims 5 has been entered in the record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 10-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al. (US 2003/0210363).

Relative to claim 1, Yasukawa et al. **teaches** an electrooptical display device (pg. 1, para 0006-0010); Yasukawa et al. further **teaches** an active matrix electrooptical display device having a plurality of display elements arranged in a matrix, (pg. 7, para. 0090 and Fig. 1), each display element including a display pixel coupled to a switch (Fig. 1, items 9a and 30); each display element including an addressable latch (Fig. 1, item 30), having an output coupled to a controlling input of the switch (pg. 7, para. 0090 and Fig. 1), the addressable latch having a row address input (gate line G1, Fig. 7) and a column address input (data input line S1, Fig. 7).

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Though the language used by Yasukawa et al. to describe the pixel structure is not exactly as that used in claims 1 and 10 of the instant invention, it would have been obvious to a person of ordinary skill in the art at the time of the invention that what is described in claims 1 and 10 of the instant invention is a general description of the pixels and controlling logic that makeup an active matrix display device, (e.g. an LCD device).

Regarding claim 11, Yasukawa et al. further **teaches** the display device wherein the addressable latch having a row electrode input and a column electrode input (Fig. 1, item 30), data input line S1 connected to the data line electrode of the latch (item 30) and the gate line G1 connected to the gate control of the pixel latch, item 30).

Regarding claim 16, Yasukawa et al. further **teaches** the display is a thin-film transistor display device (pg. 7, para. 0090).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al as applied to claim 1 in item 3 hereinabove, and further in view of Santoro et al. (US 003/0020671).

Relative to claim 4 Yasukawa et al. **does not teach** activating at least some display elements of the display device at a first refresh rate and activating other display elements of the display device at a second refresh rate, different than the first refresh rate.

Santoro et al. **teaches** a system for the simultaneous display of multiple information source (pg. 2, para. 0019 and pg. 3, paras. 0020-0024); Santoro et al. further teaches driving the first set of elements at a first refresh rate and driving the second set of elements at a second refresh rate different than the first refresh rate (pg 3, para 0020).

It would have been obvious to a person of ordinary skill in the art at the time of the invention

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to provide to the device as taught by Yasukawa et al. in view of Santoro et al. in order to put in place the means to refresh different regions or the display screen as different refresh rates in order to preserve power by using lower refresh rate when it is practical to do so.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al as applied to claim 1 in item 3 hereinabove, and further in view of Martin et al. (USP 6,094,704).

Regarding claim 12 Yasukawa et al. **does not teach** a display device wherein the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch, the row address input coupled to the row address logic, and column address input coupled to the column address logic. Martin et al. **teaches** a memory device with row and column address paths (col. 4, lines 57-67 and col. 5, lines 1-29); Martin further **teaches** a display device wherein the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch, the row address input coupled to the row address logic, and column address input coupled to the column address logic (col. 9, lines 59-64).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Yasukawa et al the feature as taught by Martin et al in order to put in place logic necessary to drive the data and gate lines which in turn activate the addressable pixel latch. It being understood by those skilled in the art that it is common practice to structure active matrix display devices with addressable logic that drives the matrix elements.

Allowable Subject Matter

6. Claims 2-3 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 2, the major difference between the teachings of the prior art of record (Yasukawa et al. (US 2003/0210363); Santoro et al. (Pub. No. US 2003/0020671) and Martin (USP 6,094,704)) and that of the instant invention is that said prior art of record **does not teach** the method steps of comparing the row address input and the row electrode input, comparing the column address input and the column electrode input, activating the display element with the logic controlled switch based on results of the comparisons.

Relative to claim 13, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display device wherein the addressable latch of each display element including first and second comparators, the first comparator having the row address input and a row electrode input, the second comparator having the column address input and a column electrode input, each display element including a logic device having a first input coupled to an output of the corresponding first comparator the logic device having a second input coupled to an input of the corresponding second comparator.

7. Claim 5, 7-9, 17 and 19-20 are allowed.

8. The following is an examiner's statement of reasons for allowance:

Relative to claim 5, the major difference between the teachings of the said prior art of record

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and that of the instant invention is that said prior art of record **does not teach** a method in a display device comprising: an $n \times m$ array of addressable display elements, the method comprising: activating at least some display elements characterizing a foreground image at a first rate; activating other display elements characterizing a background image at a second rate, the second rate less than the first rate; activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Relative to claim 17, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a method in a display device comprising an $n \times m$ array of addressable display elements, the method comprising: selectively activating display elements by individually addressing the display elements to be activated, activating the display elements includes, applying a row address input and a row electrode input to control logic of the corresponding display element, applying a column address input and a column electrode input to the control logic of the corresponding display element, and activating the display element with a logic controlled switch when the control logic inputs satisfy a condition; reducing power consumption by addressing at least some of the display elements at a first frequency and addressing other display elements at a second frequency, the second frequency less than the first frequency.

Response to Applicant's Remarks

9. Applicant's arguments filed January 17, 2007 have been fully considered but they are not persuasive.

Applicant's arguments that claims 1 and 10 fail to disclose or suggest the invention as set forth in said claim 1 and 10 is without merit. Claims 1 and 10 teach a pixel structure common in the design of active matrix display devices such as Liquid Crystal Displays.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation is found in the knowledge generally available to one of ordinary skill in the art.

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Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,476,914	Hoelzi et al.
U. S. Patent No	5,774, 104	Crossland et al.
Pub. No.	UIS 2006/0209009	Schlangen et al.

Final Action

11. This **ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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To Respond


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Vincent E. Kovalick
March 14, 2007



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